

S/N 10/783,695



PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Leonard Forbes	Examiner:	Bradley Smith
Serial No.:	10/783,695	Group Art Unit:	2824
Filed:	February 20, 2004	Docket:	1303.019US2
Title:	DRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY INSULATORS		

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicant respectfully requests that this Supplemental Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicant requests that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicant with the next official communication.

Pursuant to 37 C.F.R. §1.97(b), it is believed that no fee or statement is required with the Supplemental Information Disclosure Statement. However, if an Office Action on the merits has been mailed, the Commissioner is hereby authorized to charge the required fees to Deposit Account No. 19-0743 in order to have this Supplemental Information Disclosure Statement considered.

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Serial No :10/783,695

Filing Date: February 20, 2004

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The Examiner is invited to contact the Applicant's Representative at the below-listed telephone number if there are any questions regarding this communication.

The present application is either a U.S. national patent application filed after June 30, 2003 or an international application that entered the national stage under 35 U.S.C. § 371 after June 30, 2003. Thus, Applicant believes that the U.S. Patent & Trademark Office has waived the requirement under 37 C.F.R. 1.98 (a)(2)(i) for submitting a copy of each cited U.S. patent and each U.S. patent application publication. The waiver is provided in a pre-OG notice from the U.S. Patent & Trademark Office entitled "Information Disclosure Statements May Be Filed Without Copies of U.S. Patents and Published Applications in Patent Applications filed after June 30, 2003" and dated July 11, 2003. Applicant acknowledges the requirement to submit copies of foreign patent documents and non-patent literature in accordance with 37 C.F.R. 1.98(a)(2).

Respectfully submitted,

LEONARD FORBES

By his Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 371-2157

Date

18 November 2004

By

David R. Cochran
Reg. No. 46,632

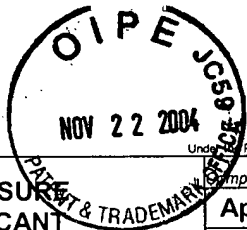
CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 18 day of November, 2004.

Name

KACIA LEE

Signature

Kacia Lee



Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Number	10/783,695
Filing Date	February 20, 2004
First Named Inventor	Forbes, Leonard
Group Art Unit	2824
Examiner Name	Smith, Bradley

Sheet 1 of 1

Attorney Docket No: 1303.019US2

US PATENT DOCUMENTS

Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Filing Date If Appropriate
	US-4,688,078	08/18/1987	Hseih, Ning	12/11/1985
	US-4,939,559	07/03/1990	DiMaria, D. J., et al.	04/01/1986
	US-5,073,519	12/01/1991	Rodder, Mark	10/31/1990
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	US-6,009,011	12/28/1999	Yamauchi, Y.	12/24/1997
	US-6,069,380	05/30/2000	Chou, Stephen Y., et al.	07/25/1997
	US-6,169,306	01/02/2001	Gardner, Mark I., et al.	07/27/1998
	US-6,238,976	05/29/2001	Noble, Wendell P., et al.	02/27/1998
	US-6,249,460	06/19/2001	Forbes, Leonard , et al.	02/28/2000
	US-6,317,364	11/13/2001	Guterman, D. C., et al.	10/13/2000
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	US-6,377,070	04/23/2002	Forbes, Leonard	02/09/2001
	US-6,514,842	02/04/2003	Prall, K. D., et al.	08/08/2001
	US-6,574,143	06/03/2003	Nakazato, Kazuo	12/08/2000
	US-6,730,575	05/04/2004	Eldridge, Jerome M.	08/30/2001
	US-6,754,108	06/22/2004	Forbes, L.	08/30/2001

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	T ²
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OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

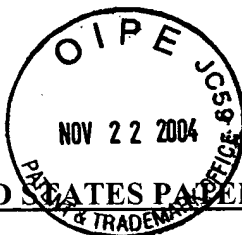
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		EIERDAL, L. , et al., "Interaction of oxygen with Ni(110) studied by scanning tunneling microscopy", <u>Surface Science</u> , 312(1-2), (June 1994), 31-53	
		MARSHALEK, R. , et al., "Photoresponse Characteristics of Thin-Film Nickel-Nickel Oxide-Nickel Tunneling Junctions", <u>IEEE Journal of Quantum Electronics</u> , QE-19(4), (1983), 743-754	

EXAMINER

DATE CONSIDERED

Substitute Disclosure Statement Form (PTO-1449)

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional) ² Applicant is to place a check mark here if English language Translation is attached



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PATENT

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Serial No.: 10/783,695
Filed: February 20, 2004
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TUNNEL BARRIER INTERPOLY INSULATORS

Examiner: Bradley Smith
Group Art Unit: 2824
Docket: 1303.019US2

COMMUNICATION CONCERNING RELATED APPLICATION(S)

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Applicant would like to bring to the Examiner's attention the following related application(s) in the above-identified patent application:

<u>Serial/Patent No.</u>	<u>Filing Date</u>	<u>Attorney Docket</u>	<u>Title</u>
09/945507	August 30, 2001	1303.014US1	FLASH MEMORY WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS
09/945395 6754108	August 30, 2001	1303.019US1	DRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY INSULATORS
09/943134	August 30, 2001	1303.020US1	PROGRAMMABLE ARRAY LOGIC OR MEMORY DEVICES WITH ASYMMETRICAL TUNNEL BARRIERS
09/945498 6778441	August 30, 2001	1303.024US1	INTEGRATED CIRCUIT MEMORY DEVICE AND METHOD
09/945512	August 30, 2001	1303.027US1	IN SERVICE PROGRAMMABLE LOGIC ARRAYS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS
09/945554	August 30, 2001	1303.028US1	SRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY INSULATORS

COMMUNICATION CONCERNING RELATED APPLICATIONS

Serial Number: 10/783,695

Filing Date: February 20, 2004

Title: DRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY INSULATORS

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09/945500	August 30, 2001	1303.029US1	PROGRAMMABLE MEMORY ADDRESS AND DECODE CIRCUITS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS
10/028001	December 20, 2001	1303.035US1	PROGRAMMABLE ARRAY LOGIC OR MEMORY WITH P-CHANNEL DEVICES AND ASYMMETRICAL TUNNEL BARRIERS
10/081818	February 20, 2002	1303.045US1	ATOMIC LAYER DEPOSITION OF METAL OXIDE AND/OR LOW ASYMMETRICAL TUNNEL BARRIER INTERPOLY INSULATORS
10/177096	June 21, 2002	1303.063US1	GRADED COMPOSITION METAL OXIDE TUNNEL BARRIER INTERPOLY INSULATORS
10/789038	February 27, 2004	1303.024US2	INTEGRATED CIRCUIT MEMORY DEVICE AND METHOD
10/781035	February 18, 2004	1303.063US2	GRADED COMPOSITION METAL OXIDE TUNNEL BARRIER INTERPOLY INSULATORS
10/929916	August 30, 2004	1303.035US2	PROGRAMMABLE ARRAY LOGIC OR MEMORY WITH P-CHANNEL DEVICES AND ASYMMETRICAL TUNNEL BARRIERS
10/788810	February 27, 2004	1303.027US2	IN SERVICE PROGRAMMABLE LOGIC ARRAYS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS
10/819550	April 7, 2004	1303.019US3	DRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY INSULATORS
10/931704	September 1, 2004	1303.014US2	FLASH MEMORY WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS

COMMUNICATION CONCERNING RELATED APPLICATIONS

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Filing Date: February 20, 2004

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10/929986	August 30, 2004	1303.045US2	ATOMIC LAYER DEPOSITION OF METAL OXIDE AND/OR LOW ASYMMETRICAL TUNNEL BARRIER INTERPOLY INSULATORS
10/931711	September 1, 2004	1303.029US2	PROGRAMMABLE MEMORY ADDRESS AND DECODE CIRCUITS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS
10/931540	August 31, 2004	1303.020US2	PROGRAMMABLE ARRAY LOGIC OR MEMORY DEVICES WITH ASYMMETRICAL TUNNEL BARRIERS

Respectfully submitted,

LEONARD FORBES

By Applicant's Representatives,

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Date 18 November 2004

By

David R. Cochran

Reg. No. 46,632

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Name

KACIA LEE

Signature

Kacia Lee